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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/617,049	07/14/2000	Won Geun Jung	2950-164P	6161

2292 7590 09/30/2003

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EXAMINER
NGUYEN, MIKE

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/30/2003

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/617,049	Applicant(s) JUNG ET AL.	
	Examiner Mike Nguyen	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Notices & Remarks

1. Applicant's amendment file on 07/09/2003 in response to Examiner's Office Action has been reviewed. The following rejections now apply.

2. Claims 1-26 are pending for the examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-3, 5-6, and 9-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui (U.S. Pat. No. 5,999,505) further in view of Kurihara et al. (U.S. Pat. No. 6,516,359 B1)

4. As to claim 1, Yasui teaches a audio data receiving apparatus (see figure 3 element 12), comprising:

a converter converting a digital audio signal into record-formatted audio data (see figure 3 element 12 and column 4 lines 33-38); and

an interface transferring (see figure 3 element 10), via a bus (see figure 3 element 100), the record-formatted audio data to a disk recording/reproducing device (see figure 3 element 8 and column 4 lines 27-32) without conducting a preparation process for transferring data when a record request is received from the disk recording/reproducing device, wherein the preparation process is specified in a bus standard protocol for a personal computer (see figure 9 and column 9 lines 53-67 and column 10 lines 1-20).

Although the apparatus as taught by the Yasui shows substantial features of the claimed invention (discussed above), it fails to teach: converting a digital audio signal, input from a source external to the audio data receiving apparatus, into record-formatted audio data. Kurihara; however, teaches a converter converting a digital audio signal, input from a source external to the audio data receiving apparatus, into record-formatted audio data (see fig. 2 element 707 and col. 7 lines 5-10 and col. 11 lines 60-67). Given the teaching of Kurihara, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Yasui by employing the well know or conventional feature of the apparatus, such as taught by Kurihara, in order to provide faster record and reduce delay in recording data onto the disk recording/reproducing device.

5. As per claims 2, 6, 13 and 16, Yasui fails to explicit to teach AT Attachment Packet Interface (ATAPI) protocol. Kurihara; however, said bus standard protocol is AT Attachment Packet Interface (ATAPI) protocol (see col. 10 lines 6-9). Given the teaching of Kurihara, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Yasui by employing the well know or conventional feature of the apparatus, such as taught by Kurihara, in order to reduce delay in recording date onto the disk recording/reproducing device.

6. As to claim 3, Yasui teaches the apparatus set forth in claim 1, further comprising a sampler converting an analog audio signal into the digital audio signal (see column 4 lines 33-38).

7. As to claim 5, Yasui teaches an audio data recording apparatus (see figure 4), comprising: a connector sending/receiving signals through a bus (see figure 4 elements 10, 100 and

column 7 lines 1-12);

a recorder modulating audio data received through said connector into recording signals and recording the recording signals in a recording medium (see figure 4 elements 818, 804 and column 6 lines 55-67 and column 7 lines 1-12); and

a controller controlling the connector to transmit a transfer start signal to a counter part of the bus without sending/receiving packet commands through the bus when a record command is received (see figure 4 element 820 and column 7 lines 1-12 and figure 9 and column 9 lines 55-67 and column 10 lines 1-20).

Although the audio data recording apparatus as taught by Yasui shows substantial features of the claimed inventions (discussed above), it fails to teach: a bus protocol compatible with a bus protocol specified for use in a personal computer. Kurihara; however, teaches a connector sending/receiving signals through a bus in accordance with a bus protocol compatible with a bus protocol specified for use in a personal computer (see fig. 2 element 707 and col. 7 lines 5-10 and col. 11 lines 60-67). Given the teaching of Kurihara, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Yasui by employing the well know or conventional feature of the apparatus, such as taught by Kurihara, in order to provide faster record and reduce delay in recording data onto the disk recording/reproducing device.

8. As to claim 9, Yasui teaches a method for sending/receiving audio data through a bus (see figures 3 element 100) comprising the steps of:

(a) entering into a data communication mode without conducting a preparation process

for transferring data over a bus when a record request is received, wherein the preparation process includes occupying a bus and issuing packet commands (see column 7 lines 1-12 and figure 9 and column 9 lines 53-67 and column 10 lines 1-20);

(b) sending/receiving audio data in the data communication mode (see figure 3 element 12 and column 4 lines 33-38); and

(c) stopping the data communication mode when a recording stop request is received (see column 10 lines 48-61 wherein the DMAC 6 will send an interruption signal to the MPU 2 when it completes the transmission or it receives a recording stop request. In response to the interruption signal the MPU 2 instructs the recording/reproducing either stopped or continued).

Although the audio data recording apparatus as taught by Yasui shows substantial features of the claimed inventions (discussed above), it fails to teach: specified in a bus standard protocol for a personal computer. Kurihara; however, teaches the preparation is specified in a bus standard protocol for a personal computer (see fig. 2 element 707 and col. 7 lines 5-10 and col. 11 lines 60-67). Given the teaching of Kurihara, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Yasui by employing the well know or conventional feature of the apparatus, such as taught by Kurihara, in order to provide faster record and reduce delay in recording data onto the disk recording/reproducing device.

9. As to claim 10, Yasui fails to explicit teach a transfer start signal. Kurihara; however, teaches transferring from a data, a receiving part to a data transferring part, via the bus, a transfer start signal without conducting the preparation process when the record request is received. Kurihara; however, teaches transferring from a data, a receiving part to a data transferring part,

via the bus, a transfer start signal without conducting the preparation process when the record request is received (see col. 6 lines 24-31 and fig. 2 element 707 and col. 7 lines 5-10 and col. 11 lines 60-67). Given the teaching of Kurihara, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Yasui by employing the well know or conventional feature of the apparatus, such as taught by Kurihara, in order to provide faster record and reduce delay in recording data onto the disk recording/reproducing device.

10. As to claim 11, Yasui teaches the method set forth in claim 10, wherein said step (c) discontinues transfer of the transfer start signal (see column 10 lines 48-61).

11. As to claim 12, Yasui teaches the method set forth in claim 9, further comprising:

(d) interrupting a data transfer operation over the bus in the data communication mode when step (c) stop the data communication mode (see column 10 lines 48-61).

12. As to claim 14, Yasui teaches the method set forth in claim 9, wherein said step (a) simultaneously transmits a transfer start signal and a command requesting start of format conversion of a received audio signal from a data receiving part to a data transferring part (see column 7 lines 1-12 and column 9 lines 53-67 and column 10 lines 1-20).

13. As to claim 15, Yasui teaches a method for sending/receiving data between two devices through a bus, comprising the steps of:

(a) simultaneously transferring a transfer start signal and a conversion start signal to a data transfer device without conducting a preparation process for transferring data when a record request is received, wherein the preparation process includes occupying the bus and issuing packet commands (see column 7 lines 1-12 and figure 9 and column 9 lines 53-67 and column 10 lines 1-20);

(b) converting an input signal into data streams of predetermined format when the data transfer device receives the conversion start signal (see col. 5 lines 33-67 and col. 5 lines 1-13);

(c) checking whether the transfer start signal is received when a predetermined number of data are generated (see col. 5 lines 33-67 and col. 5 lines 1-13); and

(d) transferring the data streams to a receiving device through the bus when step (c) indicates the transfer start signal has been received (see col. 5 lines 33-67 and col. 5 lines 1-13).

Although the method for sending/receiving data between two device through a bus as taught by Yasui shows substantial features of the claimed invention (discussed above), it fails to teach a transfer start signal. Kurihara; however, teaches a transfer start signal (see col. 6 lines 24-31 and fig. 2 element 707 and col. 7 lines 5-10 and col. 11 lines 60-67). Given the teaching of Kurihara, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Yasui by employing the well know or conventional feature of the apparatus, such as taught by Kurihara, in order to provide faster record and reduce delay in recording data onto the disk recording/reproducing device.

14. As to claim 17, Yasui fails to teaches the transfer start signal via the bus and sends the conversion start signal through a signal path different from the bus.

15. As to claim 18, Yasui teaches the method set forth in claim 15, further comprising:

(e) receiving the transferred data through the bus (see col. 4 lines 15-67 and col. 5 lines 1-13); and

(f) recording the received data (see col. 4 lines 15-67 and col. 5 lines 1-13).

16. As per claims 19, 21, 23 and 25, Yasui fails to teach: first sending a start signal, signaling to start a data transfer operation, through an AT attachment packet interface (ATAPI) protocol bus; second sending a conversion start signal, signaling to convert data into a format for transfer over the bus, through a connection other than the bus; and receiving data through the bus in accordance with the start signal and the conversion start signal. Kurihara; however, teaches: first sending a start signal, signaling to start a data transfer operation, through an AT attachment packet interface (ATAPI) protocol bus; second sending a conversion start signal, signaling to convert data into a format for transfer over the bus, through a connection other than the bus; and receiving data through the bus in accordance with the start signal and the conversion start signal (see col. 6 lines 24-31 and fig. 2 element 707 and col. 7 lines 5-10 and col. 11 lines 60-67). Given the teaching of Kurihara, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Yasui by employing the well know or conventional feature of the apparatus, such as taught by Kurihara, in order to provide faster record and reduce delay in recording data onto the disk recording/reproducing device.

17. As per claims 20, 22, 24 and 26, Yasui teaches the start signal at substantially the same times (see col. 8-20).

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Yasui and Kurihara as applied to claim 1 above, and further in view of Fujita et al. (U.S. Pat. No. 5,365,467).

As to claim 4, Yasui teaches the apparatus set forth in claim 1, wherein said interface comprises: a serial-to-parallel converter converting the record-formatted serial data into parallel data and outputting parallel data with a data writing pulse (see figure 3 element 12 and column 9

lines 55-67 and column 10 lines 1-7 wherein an audio data input is serially inputted into the converter 12 and parallel outputted from the converter 12); a memory controller (see figure 3 element 6 and column 4 lines 43-51) sequentially storing data in a memory whenever the data writing pulse is received (see figure 3 element 4 column 9 lines 55-67 and column 10 lines 1-7); and a transmitter transmitting the data to the disk recording/reproducing device through the bus when the transfer-ready signal is received (see figure 3 element 6 and figure 9 and column 9 lines 55-67 and column 10 lines 1-7 wherein the DMAC 6 is used to transmit the data to the disk recording/reproducing device 8);

Although the apparatus as taught by Yasui shows substantial features of the claimed invention (discussed above), it fails to explicitly teach: 8-bit parallel data and outputting 8-bit parallel data; and retrieving the stored 8-bit parallel data as 16-bit parallel data and simultaneously generating a transfer-ready signal when a predetermined amount of 8-bit parallel data has been stored in the memory. Fujita; however, teaches a serial-to-parallel converter converting the record-formatted serial data into 8-bit parallel data and outputting 8-bit parallel data with a data writing pulse; a memory controller sequentially storing the 8-bit parallel data in a memory whenever the data writing pulse is received, and retrieving the stored 8-bit parallel data as 16-bit parallel data and simultaneously generating a transfer-ready signal when a predetermined amount of 8-bit parallel data has been stored in the memory; and a transmitter transmitting the 16-bit parallel data to the disk recording/reproducing device through the bus when the transfer-ready signal is received (see figure 4 and column 7 lines 13-68 and column 8 lines 1-19). Given the teaching of Fujita, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Yasui and

Kurihara by employing the well know or conventional feature of the apparatus, such as taught by Fujita, in order to provide faster record and reduce delay in recording data onto the disk recording/reproducing device.

19. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Yasui and Kurihara as applied to claim 5 above, and further in view of Scheffler (U.S. Pat. No. 6,263,154 B1).

As per claims 7 and 8, the combination of Yasui and Kurihara fails to explicitly teach: changed a binary level of the transfer start signal for the counter part to start data transfer, and restored the binary level of the transfer start signal when a record stop is requested. Scheffler; however, teaches said controller changes a binary level of the transfer start signal for the counter part to start data transfer, and said controller restores the binary level of the transfer start signal when a record stop is requested (see figure 11 and column 7 lines 65-67 and column 8 lines 1-8). Given the teaching of Scheffler, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Yasui and Kurihara by employing the well know or conventional feature of the audio data recording apparatus, such as taught by Scheffler, in order to reduce delay in recording data onto the disk recording/reproducing device.

Response to Arguments

20. Applicant's arguments with respect to claim 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is (703) 305-5040 or e-

mail is mike.nguyen@uspto.gov. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

The appropriate fax number for the organization where this application or proceeding is assigned is (703) 746-7240.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Jeffrey Gaffin, can be reached on (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

Mike Nguyen
Patent Examiner
Group Art Unit 2182

09/22/2003

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
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